Google Scholar BETA

Web Images Video News Maps more »

ARM OR AMD OR Globespan exception nons Search

Advanced Scholar Search
Scholar Preferences
Scholar Help

Scholar All articles - Recent articles Results 1 - 10 of about 115 for ARM OR AMD OR Globespan

Apparatus and method for controlling access to a memory - all 2 versions »
DH Mansell, MR Nonweiler, PG Middleton - US Patent 7,171,539, 2007 - Google Patents
... Robert Nonweiler, Cambridge (GB); Peter Guy Middleton, Mougins (FR) (73) Assignee: ARM Limited, Cambridge (GB ... GENERATE CPRS VIOLATION EXCEPTION ... NON-SECURE MODE ...
Cited by 1 - Related Articles - Web Search

Security mode switching via an exception vector - all 4 versions »
SC Watt, CB Dornan, L Orion, N Chaussade, L Beinet ... - US Patent 7,305,712, 2007 - Google Patents
... (73) Assignee: ARM Limited, Cambridge ... between a secure mode and a non- secure mode under control ... at a location specified by an exception vector associated with ...
Related Articles - Web Search

Vectored interrupt control within a system having a secure domain and a non-secure domain - all 4 versions »
SC Watt, CB Dornan, L Orion, N Chaussade, L Beinet ... - US Patent 7,117,284, 2006 - Google Patents
... (73) Assignee: ARM Limited, Cambridge (GB) ... EXTERNAL PIN FIG. 16 INSTRUCTION ATTEMPTING GPRS -^ MONITOR ? GENERATE GPRS VIOLATION EXCEPTION ... NON-SECURE MODE ...
Related Articles - Web Search

Virtual to physical memory address mapping within a system having a secure domain and a non-secure ... - all 8 versions »
SC Watt, CB Dornan, L Orion, N Chaussade, L Beinet ... - US Patent 7,124,274, 2006 - Google Patents
... (73) Assignee: Arm Limited, Cambridge (GB) ... FIG. 16 INSTRUCTION ATTEMPTING CPRS -» MONITOR ? GENERATE CPRS VIOLATION EXCEPTION ... TASK A< NON-SECURE MODE TASK B < ...
Web Search

Technique for accessing memory in a data processing apparatus - all 3 versions »
L Beinet, DH Mansell, SC Watt - US Patent 7,185,159, 2007 - Google Patents
... (73) Assignee: Arm Limited, Cambridge (GB) ... FIG. 16 INSTRUCTION ATTEMPTING GPRS -> MONITOR ? GENERATE GPRS VIOLATION EXCEPTION ... TASK A< NON-SECURE MODE TASK B < ...
Related Articles - Web Search

Function control for a processor - all 3 versions »
SC Watt, L Orion, N Chaussade - US Patent 7,231,476, 2007 - Google Patents
... ARM Limited, Cambridge (GB) Subject to any disclaimer, the term ofthis ... GENERATE GPRS VIOLATION EXCEPTION ... NON-SECURE MODE MONITOR MODE (INTERRUPTS DISABLED) ...
Related Articles - Web Search

Access control in a data processing apparatus - all 2 versions »
AD Tune, PJ Aldworth, SC Watt, L Beinet, DH ... - US Patent 7,149,862, 2006 - Google Patents
... (73) Assignee: ARM Limited, Cambridge (GB) ... GENERATE GPRS VIOLATION EXCEPTION ... NON-SECURE
MODE MONITOR MODE (INTERRUPTS DISABLED) TASK A < TASK A< SMI ...
Related Articles - Web Search

Control of access to a memory by a device - all 2 versions »
SC Watt, L Beinet, DH Mansell, N Chaussade, PG ... - US Patent 7,305,534, 2007 - Google Patents

... (73) Assignee: Arm Limited, Cambridge (GB) ... FIG. 16 INSTRUCTION ATTEMPTING GPRS -> MONITOR ? GENERATE CPRS VIOLATION EXCEPTION ... NON-SECURE MODE ...
Related Articles - Web Search

Implementing Embedded Security on Dual-Virtual-CPU Systems - all 3 versions »
P Wilson, A Frey, T Mihm, D Kershaw, T Alves - IEEE Design & Test of Computers, 2007 - doi.ieeecomputersociety.org
... ARM TrustZone technology builds on the standard user-privilege ... From the nonsecure state, the CPU can enter ... through monitor mode when an exception is trapped ...
Web Search - BL Direct

Virtual machines for distributed real-time systems
M Cereia, IC Bertolotti - Computer Standards & Interfaces, 2007 - Elsevier
... the sixth version of the ARM architecture and ... enters the monitor mode from the non-secure state through ... In particular, several exception sources (IRQ, FIQ, and ...
Related Articles - Web Search

Key authors: S Ravi - A Raghunathan - S Watt - P Karger - S Chakradhar

Gooooooooooogle ▶
Result Page: 1 2 3 4 5 6 7 8 9 10 Next

Google Scholar BETA

Web Images Video News Maps more »

ARM OR AMD OR Globespan exception nons Search

Advanced Scholar Search
Scholar Preferences
Scholar Help

Scholar All articles - Recent articles Results 1 - 10 of about 115 for ARM OR AMD OR Globespan

Apparatus and method for controlling access to a memory - all 2 versions »
DH Mansell, MR Nonweiler, PG Middleton - US Patent 7,171,539, 2007 - Google Patents
... Robert Nonweiler, Cambridge (GB); Peter Guy Middleton, Mougins (FR) (73) Assignee: ARM Limited, Cambridge (GB ... GENERATE CPRS VIOLATION EXCEPTION ... NON-SECURE MODE ...
Cited by 1 - Related Articles - Web Search

Security mode switching via an exception vector - all 4 versions »
SC Watt, CB Dornan, L Orion, N Chaussade, L Beinet ... - US Patent 7,305,712, 2007 - Google Patents
... (73) Assignee: ARM Limited, Cambridge ... between a secure mode and a non- secure mode under control ... at a location specified by an exception vector associated with ...
Related Articles - Web Search

Vectored interrupt control within a system having a secure domain and a non-secure domain - all 4 versions »
SC Watt, CB Dornan, L Orion, N Chaussade, L Beinet ... - US Patent 7,117,284, 2006 - Google Patents
... (73) Assignee: ARM Limited, Cambridge (GB) ... EXTERNAL PIN FIG. 16 INSTRUCTION ATTEMPTING GPRS -^ MONITOR ? GENERATE GPRS VIOLATION EXCEPTION ... NON-SECURE MODE ...
Related Articles - Web Search

Virtual to physical memory address mapping within a system having a secure domain and a non-secure ... - all 8 versions »
SC Watt, CB Dornan, L Orion, N Chaussade, L Beinet ... - US Patent 7,124,274, 2006 - Google Patents
... (73) Assignee: Arm Limited, Cambridge (GB) ... FIG. 16 INSTRUCTION ATTEMPTING CPRS -» MONITOR ? GENERATE CPRS VIOLATION EXCEPTION ... TASK A< NON-SECURE MODE TASK B < ...
Web Search

Technique for accessing memory in a data processing apparatus - all 3 versions »
L Beinet, DH Mansell, SC Watt - US Patent 7,185,159, 2007 - Google Patents
... (73) Assignee: Arm Limited, Cambridge (GB) ... FIG. 16 INSTRUCTION ATTEMPTING GPRS -> MONITOR ? GENERATE GPRS VIOLATION EXCEPTION ... TASK A< NON-SECURE MODE TASK B < ...
Related Articles - Web Search

Function control for a processor - all 3 versions »
SC Watt, L Orion, N Chaussade - US Patent 7,231,476, 2007 - Google Patents
... ARM Limited, Cambridge (GB) Subject to any disclaimer, the term ofthis ... GENERATE GPRS VIOLATION EXCEPTION ... NON-SECURE MODE MONITOR MODE (INTERRUPTS DISABLED) ...
Related Articles - Web Search

Access control in a data processing apparatus - all 2 versions »
AD Tune, PJ Aldworth, SC Watt, L Beinet, DH ... - US Patent 7,149,862, 2006 - Google Patents
... (73) Assignee: ARM Limited, Cambridge (GB) ... GENERATE GPRS VIOLATION EXCEPTION ... NON-SECURE
MODE MONITOR MODE (INTERRUPTS DISABLED) TASK A < TASK A< SMI ...
Related Articles - Web Search

Control of access to a memory by a device - all 2 versions »
SC Watt, L Beinet, DH Mansell, N Chaussade, PG ... - US Patent 7,305,534, 2007 - Google Patents

... (73) Assignee: Arm Limited, Cambridge (GB) ... FIG. 16 INSTRUCTION ATTEMPTING GPRS -> MONITOR ? GENERATE CPRS VIOLATION EXCEPTION ... NON-SECURE MODE ...
Related Articles - Web Search

Implementing Embedded Security on Dual-Virtual-CPU Systems - all 3 versions »
P Wilson, A Frey, T Mihm, D Kershaw, T Alves - IEEE Design & Test of Computers, 2007 - doi.ieeecomputersociety.org
... ARM TrustZone technology builds on the standard user-privilege ... From the nonsecure state, the CPU can enter ... through monitor mode when an exception is trapped ...
Web Search - BL Direct

Virtual machines for distributed real-time systems
M Cereia, IC Bertolotti - Computer Standards & Interfaces, 2007 - Elsevier
... the sixth version of the ARM architecture and ... enters the monitor mode from the non-secure state through ... In particular, several exception sources (IRQ, FIQ, and ...
Related Articles - Web Search

Key authors: S Ravi - A Raghunathan - S Watt - P Karger - S Chakradhar

Gooooooooooogle ▶
Result Page: 1 2 3 4 5 6 7 8 9 10 Next

Google Scholar BETA

Web Images Video News Maps more »

exception vector OR table nonsecure mode 1996 - 2002 Search

Scholar All articles - Recent articles Results 1 - 10 of about 110 for exception vector OR table non

Security Paradigm for Mobile Terminals - all 3 versions »
E Auslander, J Azema, A Chateau, L Hamon - The Application of Programmable DSPs in Mobile ..., 2002 - doi.wiley.com
... In fact, with the exception of the access to ... An indirection table for interrupt vectors is located in ... If interrupt occurs in non-secure mode, then the program ...
Web Search

[PDF] BY ORDER OF THE COMMANDER TRAVIS AIR FORCE BASE - all 2 versions »
TAIRF BASE - Personnel, 1999 - e-publishing.af.mil
... in the local traf- fic pattern, Radar Approach Control will vector the aircraft ... Table 10.9. ... authority is limited to those items listed in the exception to AFI ...
Related Articles - View as HTML - Web Search

[PDF] National Security/Emergency Preparedness and Disaster Recovery Communications Via ACTS - all 2 versions »
CR Pasqualino, BS Abbe, F Dixon - 1996 - trs-new.jpl.nasa.gov
... of the communications link with the exception of call ... Mobile Secure Communications Experiment listed in Table 3-2 ... type are plotted for the non-secure calls only ...
View as HTML - Web Search - BL Direct

[CITATION] Network access to multi-level secure databases from desktop clients
JA Backa - 1997 - University of New Brunswick
Web Search

Distributed management with mobile components - all 2 versions »
M Feridun, W Kasteleijn, J Krause - Integrated Network Management, 1999. Distributed Management ..., 1999 - ieeexplore.ieee.org
... DMN is non-secure, or HTTPS if operating in secure ... forwarding, remote method invocation and exception forwarding ... by creating the equivalent RMON MIB table entries ...
Cited by 43 - Related Articles - Web Search

A framework for distributed management with mobile components - all 2 versions »
M Feridun, J Krause - Computer Networks, 2001 - Elsevier
... settings, eg, the default route in the routing table. ... or FTP if the DMN is non-secure, or HTTPS ... for- warding, remote method invocation and exception forwarding ...
Cited by 14 - Related Articles - Web Search

Information processing method, inter-task communication method, and computer-executable program for ... - all 6 versions »
M Sueyoshi - EP Patent 1,176,507, 2002 - freepatentsonline.com
... In other words, a security access violation exception occurs regarding an ... secure memory block 5b and the non-secure memory block ... 1, as shown in the table in Fig ...
Related Articles - Cached - Web Search

[PDF] Internet Draft Russell Dietz Hifn, Inc. Robert Cole AT&T Labs August 13, 2002 - all 3 versions »
TPM MIB - Transport, 2002 - tools.ietf.org

... Page 3. INTERNET DRAFT TPM MIB August 13, 2002 3. Table of Contents 1. Copyright Notice . . . . 2 3. Table of Contents . . . .
Related Articles - View as HTML - Web Search

Authority reduction and restoration method providing system integrity for subspace groups and single ... - all 2 versions »
KE Plambeck - US Patent 5,745,676, 1998 - freepatentsonline.com
... case BSG uses the prior-art nonsecure method of ... BASTEO) in the dispatchable unit control table (DUCT) for ... the BSG is not allowed, and an exception is signalled ...
Related Articles - Cached - Web Search

System and method for porting a multithreaded program to a job model - all 2 versions »
GM Blazo, KD Hall, C Meng, KA Streifert - US Patent 6,272,518, 2001 - freepatentsonline.com
... sockets layer (SSL) and a non-secure port 202 ... END osthread.c (180-186) **** TABLE 8B Thread ... code if /* we take an exception */ } else if ...
Cited by 4 - Related Articles - Cached - Web Search

Key authors: M Feridun - J Krause - K Moore - E Kirshenbaum - B Bareis

Gooooooooooogle ▶
Result Page: 1 2 3 4 5 6 7 8 9 10 Next

Google Scholar BETA

Web Images Video News Maps more »

ARM OR AMD OR Globespan exception vect Search

Advanced Scholar Search
Scholar Preferences
Scholar Help

Scholar All articles - Recent articles Results 1 - 10 of about 54 for ARM OR AMD OR Globespan ex

Apparatus and method for controlling access to a memory - all 2 versions »
DH Mansell, MR Nonweiler, PG Middleton - US Patent 7,171,539, 2007 - Google Patents
... Peter Guy Middleton, Mougins (FR) (73) Assignee: ARM Limited, Cambridge ... is then operable to cause predetermined tables in the ... GENERATE CPRS VIOLATION EXCEPTION ...
Cited by 1 - Related Articles - Web Search

Security mode switching via an exception vector - all 4 versions »
SC Watt, CB Dornan, L Orion, N Chaussade, L Beinet ... - US Patent 7,305,712, 2007 - Google Patents
... (73) Assignee: ARM Limited, Cambridge ... between a secure mode and a non- secure mode under control ... at a location specified by an exception vector associated with ...
Related Articles - Web Search

Vectored interrupt control within a system having a secure domain and a non-secure domain - all 4 versions »
SC Watt, CB Dornan, L Orion, N Chaussade, L Beinet ... - US Patent 7,117,284, 2006 - Google Patents
... (73) Assignee: ARM Limited, Cambridge (GB) ... EXTERNAL PIN FIG. 16 INSTRUCTION ATTEMPTING GPRS -^ MONITOR ? GENERATE GPRS VIOLATION EXCEPTION ... NON-SECURE MODE ...
Related Articles - Web Search

Virtual to physical memory address mapping within a system having a secure domain and a non-secure ... - all 8 versions »
SC Watt, CB Dornan, L Orion, N Chaussade, L Beinet ... - US Patent 7,124,274, 2006 - Google Patents
... (73) Assignee: Arm Limited, Cambridge ... translation table base address register and a secure transla -tion table base address ... GENERATE CPRS VIOLATION EXCEPTION ...
Web Search

Enhanced exception handling - all 2 versions »
EP Patent 1,865,435, 2007 - freepatentsonline.com
... in systems having the ARM ® TrustZone ® architecture ... RAM 64, accessible in non-secure mode, and a ... an exception handler 94, an exception vector table 95 and a ...
Cached - Web Search

Technique for accessing memory in a data processing apparatus - all 3 versions »
L Beinet, DH Mansell, SC Watt - US Patent 7,185,159, 2007 - Google Patents
... (73) Assignee: Arm Limited, Cambridge (GB) ... FIG. 16 INSTRUCTION ATTEMPTING GPRS -> MONITOR ? GENERATE GPRS VIOLATION EXCEPTION ... TASK A< NON-SECURE MODE TASK B < ...
Related Articles - Web Search

Implementing Embedded Security on Dual-Virtual-CPU Systems - all 3 versions »
P Wilson, A Frey, T Mihm, D Kershaw, T Alves - IEEE Design & Test of Computers, 2007 - doi.ieeecomputersociety.org
... ARM TrustZone technology builds on the standard user ... the rich operating system controls the normal vector table. ... monitor mode when an exception is trapped into ...
Web Search - BL Direct

Function control for a processor - all 3 versions »
SC Watt, L Orion, N Chaussade - US Patent 7,231,476, 2007 - Google Patents

... ARM Limited, Cambridge (GB) ... SECURE TNON-SECURE PAGE TABLE WALK Ii MAIN TUB CONTAINS THE VALID TAGGED SECURE DESCRIPTOR ... GENERATE GPRS VIOLATION EXCEPTION ...
Related Articles - Web Search

Virtual machines for distributed real-time systems
M Cereia, IC Bertolotti - Computer Standards & Interfaces, 2007 - Elsevier
... of this register to locate the exception vector table whenever the ... the sixth version of the ARM architecture and ... Yet another exception table is used for the ...
Related Articles - Web Search

Secure mode for processors supporting interrupts - all 2 versions »
F Dahan, C Roussel, A Chateau, P Cumming - US Patent 7,237,081, 2007 - Google Patents
... the Digital World; ARM926EJ-S Jazelle-Enhanced Microcell, www.arm.com/armtech ... EXIT STATUS^"EXCEPTION" ... vector table and interrupt service routines are not trusted ...
Related Articles - Web Search

Key authors: S Watt - D Mansell - N Chaussade - L Belnet - E Gallery

Gooooooogle ▶
Result Page: 1 2 3 4 5 6 Next

Google Scholar BETA

Web Images Video News Maps more »

ARM OR AMD exception vector table nonsecu Search

Advanced Scholar Search
Scholar Preferences
Scholar Help

Scholar All articles - Recent articles Results 1 - 10 of about 53 for ARM OR AMD exception vector

Did you mean: ARM OR *AND* exception vector table nonsecure mode switch OR monitor

Apparatus and method for controlling access to a memory - all 2 versions »
DH Mansell, MR Nonweiler, PG Middleton - US Patent 7,171,539, 2007 - Google Patents
... Peter Guy Middleton, Mougins (FR) (73) Assignee: ARM Limited, Cambridge ... is then operable to cause predetermined tables in the ... GENERATE CPRS VIOLATION EXCEPTION ...
Cited by 1 - Related Articles - Web Search

Xen on ARM: System Virtualization Using Xen Hypervisor for ARM-Based Secure Mobile Phones
JY Hwang, SB Suh, SK Heo, CJ Park, JM Ryu, SY Park ... - Consumer Communications and Networking Conference, 2008. ..., 2008 - ieeexplore.ieee.org
... Secure and nonsecure guest Linux virtual machines are ... handling that makes CPU to jump into exception vector table. ... sensitive registers such as ARM's FAR ...
Cited by 1 - Related Articles - Web Search

Security mode switching via an exception vector - all 4 versions »
SC Watt, CB Dornan, L Orion, N Chaussade, L Beinet ... - US Patent 7,305,712, 2007 - Google Patents
... (73) Assignee: ARM Limited, Cambridge ... between a secure mode and a non- secure mode under control ... at a location specified by an exception vector associated with ...
Related Articles - Web Search

Vectored interrupt control within a system having a secure domain and a non-secure domain - all 4 versions »
SC Watt, CB Dornan, L Orion, N Chaussade, L Beinet ... - US Patent 7,117,284, 2006 - Google Patents
... (73) Assignee: ARM Limited, Cambridge (GB) ... EXTERNAL PIN FIG. 16 INSTRUCTION ATTEMPTING GPRS -^ MONITOR ? GENERATE GPRS VIOLATION EXCEPTION ... NON-SECURE MODE ...
Related Articles - Web Search

Virtual to physical memory address mapping within a system having a secure domain and a non-secure ... - all 8 versions »
SC Watt, CB Dornan, L Orion, N Chaussade, L Beinet ... - US Patent 7,124,274, 2006 - Google Patents
... (73) Assignee: Arm Limited, Cambridge ... translation table base address register and a secure transla -tion table base address ... GENERATE CPRS VIOLATION EXCEPTION ...
Web Search

Enhanced exception handling - all 2 versions »
EP Patent 1,865,435, 2007 - freepatentsonline.com
... in systems having the ARM ® TrustZone ® architecture ... of the exception handlers and exception vector tables comprise software ... the secure and non-secure modes. ...
Cached - Web Search

Technique for accessing memory in a data processing apparatus - all 3 versions »
L Beinet, DH Mansell, SC Watt - US Patent 7,185,159, 2007 - Google Patents
... (73) Assignee: Arm Limited, Cambridge (GB) ... FIG. 16 INSTRUCTION ATTEMPTING GPRS -> MONITOR ? GENERATE GPRS VIOLATION EXCEPTION ... TASK A< NON-SECURE MODE TASK B < ...
Related Articles - Web Search

Implementing Embedded Security on Dual-Virtual-CPU Systems - all 3 versions »
P Wilson, A Frey, T Mihm, D Kershaw, T Alves - IEEE Design & Test of Computers, 2007 - doi.ieeecomputersociety.org
... ARM TrustZone technology builds on the standard user ... the rich operating system controls the normal vector table. ... monitor mode when an exception is trapped into ...
Web Search - BL Direct

Enhanced Exception Handling - all 2 versions »
CGC Neveux - US Patent 20,070,283,146, 2007 - freepatentsonline.com
... in systems having the ARM® TrustZone® architecture ... the exception handlers and exception vector tables comprise software ... between the secure and non-secure modes ...
Cached - Web Search

Function control for a processor - all 3 versions »
SC Watt, L Orion, N Chaussade - US Patent 7,231,476, 2007 - Google Patents
... ARM Limited, Cambridge (GB) ... SECURE TNON-SECURE PAGE TABLE WALK Ii MAIN TUB CONTAINS THE VALID TAGGED SECURE DESCRIPTOR ... GENERATE GPRS VIOLATION EXCEPTION ...
Related Articles - Web Search

Key authors: S Watt - D Mansell - N Chaussade - L Belnet - E Gallery

Did you mean to search for: ARM OR *AND* exception vector table nonsecure mode switch OR monitor

Gooooooogle ▶
Result Page: 1 2 3 4 5 6 Next

ARM OR AMD exception vector tab Search

Google Home - About Google - About Google Scholar

Google Scholar BETA

Web Images Video News Maps more »

vector * table secure mode interrupt OR exce | 1996 - 2002 | Search

Scholar All articles - Recent articles Results 1 - 10 of about 1,400 for vector * table secure mode i

Method and apparatus for secure execution of software prior to a computer system being powered down ... - all 5 versions »
MF Angelo, CA Miller - US Patent 5,850,559, 1998 - freepatentsonline.com
... of the invention utilizes a hash table 206 containing ... on/off switch 182, the interrupt vector points to ... power supply 180 following the secure shutdown procedure ...
Cited by 20 - Related Articles - Cached - Web Search

Method and system for executing programs using memory wrap in a multi-mode microprocessor - all 3 versions »
J Letwin - US Patent 5,561,788, 1996 - Google Patents
... a segment descriptor from a descriptor table in the ... the present invention for handling vector interrupts ... three separate protection violations in protected mode. ...
Cited by 20 - Related Articles - Web Search

Method and apparatus for protecting flash memory - all 7 versions »
PE Mattison - US Patent 6,363,463, 2002 - freepatentsonline.com
... DOS programs is to modify the interrupt vector table to intercept ... system initialization process, the reset vector goes in ... to change into a secure operating mode ...
Cited by 23 - Related Articles - Cached - Web Search

Experience with TCP/IP networking protocol S/W over embedded OS for network appliance - all 3 versions »
SW Tak, JM Son, TK Kim - Proceedings of International Workshops on Parallel ..., 1999 - doi.ieeecomputersociety.org
... to enter kernel mode from user mode used in 4.4 ... of interrupt level in order to secure data integrity ... card device driver into the interrupt vector table in the ...
Cited by 13 - Related Articles - Web Search - BL Direct

Secure communication system - all 8 versions »
S Dimolitsas, RJ Ragland, F Hemmati - US Patent 5,963,621, 1999 - freepatentsonline.com
... 32 is a table for describing the Tone Index ... is neither decrypted, nor descrambled (with the exception of certain ... from the POT voice to the secure mode can, and ...
Cited by 23 - Related Articles - Cached - Web Search

Secure power supply for protecting the shutdown of a computer system - all 3 versions »
A Crisan - US Patent 5,751,950, 1998 - freepatentsonline.com
... routine in a system interrupt handling table only if ... shows a second embodiment of the secure power supply ... 174 responds by providing the interrupt vector to the ...
Cited by 12 - Related Articles - Cached - Web Search

Making Home Automation Communications Secure - all 7 versions »
P Bergstrom, K Driscoll, J Kimball - 2001 - doi.ieeecomputersociety.org
... Table 1. Communications security layer resource constraints ... The initialization vector for this message includes ... safety-critical, and secure systems' architecture ...
Cited by 26 - Related Articles - Web Search - BL Direct

Exception response table in environment services patterns - all 2 versions »

US Patent 6,339,832, 2002 - freepatentsonline.com
... a program (the polymorphic exception handler) with ... calculating a mathematical table, or solving ... distributed, interpreted, robust, secure, architecture-neutral ...
Cited by 6 - Related Articles - Cached - Web Search

Computer emulator - all 2 versions »
H Ogata, A Tanimoto, Y Nakaoka, M Kojima, Y ... - US Patent 5,758,124, 1998 - freepatentsonline.com
... Hence, it is not necessary to secure the address in advance. ... Following the step described above, corresponding interrupt vector setting table JT is ...
Cited by 5 - Related Articles - Cached - Web Search

Safe and protected execution for the Morph/AMRM reconfigurableprocessor - all 13 versions »
AA Chien, JH Byun - Field-Programmable Custom Computing Machines, 1999. FCCM'99. ..., 1999 - ieeexplore.ieee.org
... bus or defeating the tinier interrupt which ensures ... processes run in an unprivileged mode (user mode). The page tables, mapping information for each process ...
Cited by 54 - Related Articles - Web Search

Key authors: J Letwin - P Mattison - F Hemmati - P Bergstrom - A Chien

Gooooooooooogle ▶
Result Page: 1 2 3 4 5 6 7 8 9 10 Next

vector * table secure mode interrupt Search

Google Home - About Google - About Google Scholar

Google Scholar BETA

Web Images Video News Maps more »

exception vector table nonsecure mode switcl Search

Advanced Scholar Search
Scholar Preferences
Scholar Help

Scholar All articles - Recent articles Results 1 - 10 of about 149 for exception vector table nonsec

Apparatus and method for controlling access to a memory - all 2 versions »
DH Mansell, MR Nonweiler, PG Middleton - US Patent 7,171,539, 2007 - Google Patents
... memory management unit is then operable to cause predetermined tables in the ... GENERATE CPRS VIOLATION EXCEPTION ... NON-SECURE MODE MONITOR MODE (INTERRUPTS ENBLED) ...
Cited by 1 - Related Articles - Web Search

Security mode switching via an exception vector - all 4 versions »
SC Watt, CB Dornan, L Orion, N Chaussade, L Beinet ... - US Patent 7,305,712, 2007 - Google Patents
... a secure mode and a non- secure mode under control ... specified by an exception vector associated with ... SUPERVISOR MODE MONITOR MODE / UNDEF MODE SUPERVISOR MODE ...
Related Articles - Web Search

Enhanced exception handling - all 2 versions »
EP Patent 1,865,435, 2007 - freepatentsonline.com
... of the exception handlers and exception vector tables comprise software ... between the secure and non-secure modes. The monitor mode software may be programmed to ...
Cached - Web Search

Enhanced Exception Handling - all 2 versions »
CGC Neveux - US Patent 20,070,283,146, 2007 - freepatentsonline.com
... of the exception handlers and exception vector tables comprise software ... between the secure and non-secure modes. The monitor mode software may be programmed to ...
Cached - Web Search

Vectored interrupt control within a system having a secure domain and a non-secure domain - all 4 versions »
SC Watt, CB Dornan, L Orion, N Chaussade, L Beinet ... - US Patent 7,117,284, 2006 - Google Patents
... GENERATE GPRS VIOLATION EXCEPTION RUN MONITOR PROGRAM IN MONITOR MODE STARTING AT
CPSR VIOLATION ENTRY POINT ... NON-SECURE MODE MONITOR MODE (INTERRUPTS DISABLED) ...
Related Articles - Web Search

Virtual to physical memory address mapping within a system having a secure domain and a non-secure ... - all 8 versions »
SC Watt, CB Dornan, L Orion, N Chaussade, L Beinet ... - US Patent 7,124,274, 2006 - Google Patents
... table base address register and a secure transla -tion table base address ... GENERATE CPRS VIOLATION EXCEPTION ... NON-SECURE MODE MONITOR MODE (INTERRUPTS ENBLED) ...
Web Search

Implementing Embedded Security on Dual-Virtual-CPU Systems - all 3 versions »
P Wilson, A Frey, T Mihm, D Kershaw, T Alves - IEEE Design & Test of Computers, 2007 - doi.ieeecomputersociety.org
... the rich operating system controls the normal vector table. From the nonsecure state, the CPU can enter the ... through monitor mode when an exception is trapped ...
Web Search - BL Direct

Technique for accessing memory in a data processing apparatus - all 3 versions »

L Beinet, DH Mansell, SC Watt - US Patent 7,185,159, 2007 - Google Patents
... GENERATE GPRS VIOLATION EXCEPTION RUN MONITOR PROGRAM IN MONITOR MODE STARTING AT
CPSR VIOLATION ENTRY POINT ... NON-SECURE MODE ... MONITOR MODE (INTERRUPTS DISABLED) ...
Related Articles - Web Search

Virtual machines for distributed real-time systems
M Cereia, IC Bertolotti - Computer Standards & Interfaces, 2007 - Elsevier
... of this register to locate the exception vector table whenever the ... Yet another exception table is used for the exceptions ... the secure and the non-secure states,. ...
Related Articles - Web Search

Secure mode for processors supporting interrupts - all 2 versions »
F Dahan, C Roussel, A Chateau, P Cumming - US Patent 7,237,081, 2007 - Google Patents
... EXIT STATUS^"EXCEPTION" SET RETURN POINTER ... RETURN TO NON- SECURE OPERATION . 2. 031 1032 1034 ... vector table and interrupt service routines are not trusted, ...
Related Articles - Web Search

Key authors: J Ashby - C Burkhart - F Favors - R Tiemann - R Vandaveer

Gooooooooooogle ▶
Result Page: 1 2 3 4 5 6 7 8 9 10 Next

Google Scholar BETA

Web Images Video News Maps more »

exception vector table nonsecure mode switcl 1996 - 2002 Search

Scholar All articles - Recent articles Results 1 - 10 of about 17 for exception vector table nonsecu

[PDF] BY ORDER OF THE COMMANDER TRAVIS AIR FORCE BASE - all 2 versions »
TAIRF BASE - Personnel, 1999 - e-publishing.af.mil
... in the local traf- fic pattern, Radar Approach Control will vector the aircraft ... Table 10.9. ... authority is limited to those items listed in the exception to AFI ...
Related Articles - View as HTML - Web Search

Secure communication system - all 8 versions »
S Dimolitsas, RJ Ragland, F Hemmati - US Patent 5,963,621, 1999 - freepatentsonline.com
... between the provided secure and non-secure information carried ... 32 is a table for describing the Tone ... decrypted, nor descrambled (with the exception of certain ...
Cited by 23 - Related Articles - Cached - Web Search

[PDF] THE OPEN PLATFORM PROTECTION PROFILE (OP3) TAKING THE COMMON CRITERIA TO THE OUTER LIMITS - all 5 versions »
M Kekicheff, F Kashef, D Brewer, D House, F Rd - The 23rd National Information Systems Security Conference, ..., 2000 - www-08.nist.gov
... and report the nature of the exception and the ... current command as the Initial Chaining Vector (ICV) for ... components into TOE configurations (see Table 1) proved ...
Cited by 2 - Related Articles - View as HTML - Web Search

[PDF] Secure SNMP-Based Network Management in Low Bandwidth Networks - all 2 versions »
HE Hia - 2001 - scholar.lib.vt.edu
... iv Table of Contents ... inherent security capabilities, and (ii) using a non- secure version of ... top-level network management authority securely monitor the entire ...
Cited by 1 - Related Articles - View as HTML - Web Search

Apparatus and storage medium for decrypting information - all 3 versions »
R Nagel, TH Lipscomb - US Patent 5,661,799, 1997 - freepatentsonline.com
... TABLE II. ... controller, rather than the CD-ROM reader; however, with the exception of this ... (3) Add the most recent communication message (initial vector) to the ...
Cited by 2 - Related Articles - Cached - Web Search

[BOOK] Cisco Network Design Handbook
M Salvagno - 2000 - John Wiley & Sons Inc
Cited by 3 - Related Articles - Web Search

Method and apparatus for retrieving selected information from a secure information source - all 2 versions »
R Nagel, TH Lipscomb - US Patent 5,592,549, 1997 - freepatentsonline.com
... TABLE IV. ... an initial key for the key register and an initial input vector for the ... controller, rather than the CD-ROM reader; however, with the exception of this ...
Cited by 10 - Related Articles - Cached - Web Search

A new authorization model and its mechanism using service paths in open distributed systems
M Soshi, M Maekawa - Distributed Applications and Interoperable Systems, 1997 - books.google.com
... Table 1 Service sequences authorized to invoke services client ... to execute d. Only one exception to this is ... The access control vector corresponding to (OC,(u, os ...

Related Articles - Web Search

Digitally programmable multifunction radio system architecture - all 7 versions »
WC Phillips, CL Hilterbrick, RW Minarik, KM ... - US Patent 6,072,994, 2000 - freepatentsonline.com
... TABLE A. ... IFF Transpond HF AJ IFF Interrogate HF Link 11 Mode S VHF ... The indicated modular partitioning (with the minor exception discussed later) eliminates the ...
Cited by 15 - Related Articles - Cached - Web Search

[PDF] Microphone Array Phased Processing System (MAPPS) Version 4.0 Manual - all 2 versions »
ME Watts, M Mosher, M Barnes, J Bardina - NASA TM March, 1999 - ntrs.nasa.gov
... Batch Mode.....29 ... a nonsecure ... translation vector and ...
Cited by 1 - Related Articles - View as HTML - Web Search

Key authors: F Hemmati - R Nagel - R Ragland - S Dimolitsas - T Lipscomb

Google ▶
Result Page: 1 2 Next

exception vector table nonsecure mc Search

Google Home - About Google - About Google Scholar

Google Scholar BETA

Web Images Video News Maps more »

vector * table mode interrupt OR exception 1996 - 2002 Search

Scholar All articles - Recent articles Results 1 - 10 of about 29,600 for vector * table mode interrup

Protected mode simulation of a real mode interupt based programming interface in a computer system - all 2 versions »
MC Woodring, PD Crutcher - US Patent 5,603,014, 1997 - freepatentsonline.com
... reading a pointer that specifies the next interrupt service routine of the interrupt service routines from a real mode interrupt vector table for the processor ...
Cited by 11 - Related Articles - Cached - Web Search

Microprocessor with an architecture mode control capable of supporting extensions of two distinct ... - all 2 versions »
JW Goetz, SW Mahin, JJ Bergkvist - US Patent 5,854,913, 1998 - freepatentsonline.com
... when the interrupt or exception occurred ... status and control registers and interrupt vector table; ... X86 real mode and protected mode interrupt vector tables; and. ...
Cited by 23 - Related Articles - Cached - Web Search

Method and system for executing programs using memory wrap in a multi-mode microprocessor - all 3 versions »
J Letwin - US Patent 5,561,788, 1996 - Google Patents
... means for handling exist -ing real mode programs which store the address of their own interrupt handling routines into the hardware interrupt vector table. ...
Cited by 20 - Related Articles - Web Search

... output devices utilizing processor with virtual system mode by allowing mode interpreters to operate ... - all 2 versions »
DR Wooten - US Patent 5,832,239, 1998 - freepatentsonline.com
... the logical base address of the VSM interrupt vector table. ... are both accessible from any user mode until VSM ... 1" is ignored and will not produce an exception. ...
Cited by 17 - Related Articles - Cached - Web Search

Processor with virtual system mode - all 3 versions »
DR Wooten - US Patent 5,644,755, 1997 - freepatentsonline.com
... the logical base address of the VSM interrupt vector table. ... are both accessible from any user mode until VSM ... 1" is ignored and will not produce an exception. ...
Cited by 17 - Related Articles - Cached - Web Search

Integrating multi-modal synchronous interrupt handlers for computer system - all 2 versions »
MJ Corrigan, SL Jones, LW Loen, DR Russell Jr, PB ... - US Patent 5,734,910, 1998 - freepatentsonline.com
... environment-specific interrupt handler for the current task and invoke it in the hardware mode that environment expects ... Since the table is a vector, the code ...
Cited by 10 - Related Articles - Cached - Web Search

Protocol for interrupt bus arbitration in a multi-processor system - all 5 versions »
PK Nizar, D Carson - US Patent 5,696,976, 1997 - freepatentsonline.com
... _____ Vector (0:7): Identifies interrupt being sent. Delivery Mode (8:10): Same interpretation as for Re-direction Table 109. ...
Cited by 19 - Related Articles - Cached - Web Search

Method and system for transitioning the network mode of a workstation - all 2 versions »

JC Dunn, FC Foltz - US Patent 5,701,491, 1997 - freepatentsonline.com
... In other words, this portion of the transition program effectively takes a "snapshot" of the pre-real mode network interrupt vector table and stores the ...
Cited by 8 - Related Articles - Cached - Web Search

Advanced programmable interrupt controller - all 6 versions »
DA Klein... - US Patent 5,745,772, 1998 - freepatentsonline.com
... The I/O APIC module 60 can also be programmed in APIC bypass mode, in which case it ... 4A is an interrupt vector translation table which depicts the ...
Cited by 11 - Related Articles - Cached - Web Search

Interrupt control architecture for symmetrical multiprocessing system - all 2 versions »
D Gephardt, R Mahalingaiah - US Patent 5,555,430, 1996 - freepatentsonline.com
... 1 Enables the pin to be a cascaded interrupt MSK Mask 1 Interrupt is masked CM Cascade Mode 2 Cascaded Interrupt vector delivery mode - refer to Table 2 PL ...
Cited by 30 - Related Articles - Cached - Web Search

Key authors: P Nizar - D Carson - R Mahalingaiah - D Gephardt - R Srinivasan

Gooooooooooogle ▶
Result Page: 1 2 3 4 5 6 7 8 9 10 Next

vector * table mode interrupt OR ex Search

Google Home - About Google - About Google Scholar